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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
CHANG, EDITH M

ART UNIT	PAPER NUMBER
2634	9

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/382,459	DEDIC ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-29,33-38 and 40* is/are allowed.

6)☒ Claim(s) *30-32 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *16 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Hata (US Patent 5479455).

Regarding claim 30, Hata discloses a digital circuit (FIG.1) comprising: an input signal processing circuit (2 FIG.1) clocked by a first clock signal (CLK FIG.1), inputting one or more first signal(s) (Din FIG.1), and performing a predetermined processing operation on the first signal(s); a first latch circuit (9b FIG.14) clocked by a second clock signal (CLKb FIG.14), and inputting an output signal from the input signal processing circuit (Din FIG.14); a second latch circuit (9a FIG.14) clocked by a third clock signal (CLKa FIG.14), and inputting an output signal (a FIG.14) from the first latch circuit; and a clock generating circuit (6 FIG.4) generating the second and third clock signals from the first clock signal (CLKin FIG.14), the second clock signal being delayed relative to the first clock signal by a predetermined delay time (CLKb FIG.15, where the second rising edge of CLKb is delayed from the first rising edge of CLKin), and a rising edge of the third clock signal occurring at substantially a same time as a rising edge of the first clock signal (CLKa FIG.15, wherein the first rising edge of CLKa occurs substantially a same time of the first rising edge of CLKin) and enabling the second latch circuit to

enter a responsive state during a non-responsive state of the first latch circuit (CLKa & CLKb FIG.15, wherein the CLKa is high/enabled while the CLKb is low).

Regarding claim 31, Hata discloses the clock generating circuit comprises: a delay element (18 FIG.19) delaying the first clock signal (a FIG.19) to produce a delayed version thereof (c FIG.19), and a logic element (28 FIG.19) logically combining the first clock signal with a delayed version thereof such that an enabling change in the third clock signal (e FIG.19) occurs substantially simultaneously with an enabling change in the first clock signal (e & a FIG.21, where the first rising edge of e occurs substantially simultaneously with the first rising edge of a), and a disabling change in the third clock signal occurs substantially simultaneously with a change in the delayed version of the first clock signal (c & a FIG.21, where the second falling edge of e occurs substantially simultaneously with the fourth falling edge in c).

Regarding claim 32, Hata discloses clock generating circuit (6 FIG.14, FIG.19) further comprises: a delay balancing element (28-30 FIG.19) connected between said delay element (18 FIG.19) and said first latch circuit (6-9b FIG.14) receiving said delayed version of the first clock signal (c FIG.19) and deriving therefrom said second clock signal (CLKb FIG.14), and the delay balancing element having a first propagation delay between said change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal causing the first latch circuit to change from a non-responsive state to a responsive state (in FIG.21 the delay from the first falling edge of a and the first falling edge of c/delayed version is about one and one third interval, in FIG.15 the delay of enabling the CLKb/first latch is about one and one fourth interval wherein the first rising edge of CLKin to the second rising edge of CLKb,

so there is a propagation delay) , said logic element having a second propagation delay between said change in said delayed version of the first clock signal and said disabling change in the third clock signal, and said first propagation delay being substantially equal to said second propagation delay (The logical element is 28 FIG.19, the balancing element is 28-30 FIG.19, the propagation delays is substantially equal as the clock generating circuit/control signal circuit construct in 6-9b, 6-9a FIG.14 and FIG.19 the detail construction of 6 FIG.14).

3. Claim 39 is rejected under 35 U.S.C. 102(b) as being anticipated by Bechade et al. (US Patent 5272729).

Regarding claim 39, Bechade et al. discloses a digital circuit (fig.1), comprising: a digital input circuit (14 fig.1) receiving a plurality of digital signals (13 fig.1) in response to a first clock signal (EXTERNAL CLOCK fig.1); a delay element (12 fig.1) receiving the first clock signal and outputting a delayed clock signal (13 fig.1); a clock generating circuit (13-14-18-23 fig.1) receiving the first clock signal and generating a second clock signal (output of 18/input of 16 fig.1), produced from the delayed clock signal (13 fig.1), and a third clock signal (23 fig.1), produced from the first clock signal and the delayed clock signal (11'' fig.1); a first latch circuit (16 fig.1), coupled to the digital input circuit, receiving the output signal from the digital input circuit in response to the second clock signal (18 fig.1); and a second latch circuit (19 fig.1), coupled to the first latch circuit, receiving the output signal from the first latch circuit in response to the third clock signal (23 fig.1).

Allowable Subject Matter

Claims 1-29, 33-38, & 40 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4800.

Edith Chang
August 27, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600